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09/405,618	09/24/1999	JAMES S. BLOMGREN	31876.0140	9689

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EXAMINER
CRAIG, DWIN M

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/405,618
Filing Date: September 24, 1999
Appellant(s): BLOMGREN ET AL.

Karen S. Write
Mathew J. Booth
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6-04-2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1-3, 6-8, 11-13, 16-18 and 21-23 stand or fall together because appellant's brief includes a statement that this grouping of claims does stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,706,476	Giramma	1-1998
6,069,497	Blomgren et al.	5-2000

IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164), March 18, 1993, The Institute of Electrical and Electronics Engineers, Inc. New York, N.Y., ISBN 1-55937-299-0.

"On the Use of VHDL as a Multi-Valued Logic Simulator", C. Rozon, Royal Kings College, Kingston Ontario Canada, IEEE 1996.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

- **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claims 1-7, 8-14, 15-21, 22-28 and 29-35** in view of **Leight et al. U.S. Patent 6,289,497.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing a signal naming convention that describes an N-nary logic circuit. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have used the system as described in the *Leight et al.* reference to model signals in an N-nary logic simulation because, (...the tool of the present invention does not require a semiconductor designer to develop a schematic and a separate behavioral model that must be verified against each other. Instead, the design tool

of the present invention separately compiles both a behavioral model and a physical circuit description from one syntax statement. The present invention guarantees that the schematic and the behavioral model will "match up," greatly reducing the man-hours needed to design semiconductor circuits, *Leight et al. Col. 2 Lines 49-57*). Specifically the *Leight et al.* reference discloses as signal model for N-nary logic simulation ***Leight, Claim 6,*** wherein there is a signal strength field, ***Claim 2, a signal degree field,*** and a signal definition field ***Claim 4, a mux select expression, an arithmetic expression, a logical expression, a multiple output expression, a capacitance isolation expression, or a shared node expression.***

- **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by Giramma "METHOD AND APPARATUS FOR USE OF THE UNDEFINED LOGIC STATE AND MIXED MULTIPLE-STATE ABSTRACTIONS IN DIGITAL LOGIC SIMULATION" U.S. Patent 5,706,476. *Giramma* discloses, Taking as per claim(s) 1, 6, 11, 16 and 21 for example: A model that simulates logic signals capable of having more than two unique values and one or more unique drive states. Col. 1, lines 20-63 and in claim 1 *Giramma* recites, "A computer-assisted logic gate simulation method for simulating a circuit that includes plural logic gates characterized by differing output state abstractions, " whereby the unique driver states comprise: a signal value field *Giramma* discloses, "Those of skill in the art will appreciate that by directive production is meant any technique for signaling or otherwise

communicating to a downstream connected primitive the possible next-state of its inputs based upon a transition of state of an output of an upstream primitive." Col. 5, Lines 13-18. *Giramma* recites a signal strength field, "In addition to these state abstractions, some logic simulators use a 3-state model coupled with essentially unlimited strengths or values." Col. 1, Lines 51-53. *Giramma* also teaches a signal definition field which comprises information that conveys whether the signal being modeled holds a defined value or an undefined value, "Also preferably, the 4-state abstraction includes an undefined state such as undefined state XS described above." Col. 4, Lines 53-55.

- With respect to claims 2,7,12,17 and 22 *Giramma* discloses, "Those skilled in the art will appreciate that 32-bit `zoom` words, in accordance with the preferred embodiment of the invention, are used to obtain indices into various tables for next-state logic evaluations." Col. 6, Lines 51-54.
- With respect to claims 3, 8, 13, 18 and 23 *Giramma* discloses, "Multiple-Value Logic 9-state model (MVL-9) of 0, 1, X at strong and resistive strengths or values, as well as high-impedance uninitialized, and undefined (0S,1S,XS,0R,1R,XR,Z,U,D). " **Col. 1, Lines 46-49.**
- **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by the IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164). *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* discloses, with respect to claim(s) 1, 6, 11, 16 and 21, logic signals capable of having more than two

unique values and one or more unique drive states. On **Page 2,** *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* recites, SUBTYPE UX01Z IS resolved std_ulogic RANGE 'U' TO 'Z'; -- ('U','X','0','1','Z').

IEEE Standard Multivalue Logic System for VHDL Model Interoperability recites on in **Annex A on Page 15**, "A.1 Value system...one must interpret the meaning of each of the elements as provided by the standard. Type std_ulogic is ('U', Uninitialized state Used as a default value 'X', Forcing Unknown Bus contentions, error conditions, etc. '0', Forcing Zero Transistor driven to GND '1', Forcing One Transistor driven to VCC 'Z', High Impedance 3-state buffer outputs 'W', Weak Unknown Bus terminators 'L', Weak Zero Pull down resistors 'H', Weak One Pull up resistors '-' Don't Care Used for synthesis and advanced modeling); " which is a signal value field in the Multivalue Logic System as well as a signal definition field. *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* teaches on **Page 15, Annex A;** " Therefore, a number of strength stripper functions have been designed to transform 'Z', 'W', 'L', 'H', and '-' into their corresponding forcing strength counterparts." This teaches a signal strength field.

- With respect to claims 2, 3, 7, 8, 12, 13, 17, 18, 22 and 23 *IEEE Standard Multivalue Logic System for VHDL Model Interoperability* teaches on **Page 15, Annex A,** "Forcing Zero Transistor driven to GND, Forcing One Transistor driven to VCC, Weak Zero Pull Down resistors, Weak One Pull up Resistors.

- ***(This rejections is withdrawn, see the response to arguments below.)*** **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** are being rejected under 35 U.S.C. 102(b) as being clearly anticipated by "On the Use of VHDL as a Multi-Valued Logic Simulator" by C. Rozon, IEEE 1996 hereafter referred to as the **Rozon** reference.
- As regards **Claims 1, 6, 11, 16 and 21,** the *Rozen* reference teaches a signal model for an N-Nary logic simulation **Pages 110-115.** wherein the logic value comprises an integer greater than 1 **Table 1, page 110**, and a signal strength **Table 1, page 110** and signal definition **Page 112, and Table 2**.
- As regards **Claims 2, 7, 12, 17 and 22** the *Rozon* reference discloses an integer less than or equal to 31 **ANNEX 1, page 114.**
- As regards **Claims 3, 8, 13, 18 and 23** the *Rozon* reference discloses the signal strength being high-impedance, weakly-driven, moderately driven or strongly-driven, **Page 110 Table 1.**

(11) Response to Argument

On pages 7 and 8, of the Brief the Appellant has stated, *"...the Examiner has never developed an understanding of the substantial difference between the Assignee's nonbinary FAST 14 technology and the modeling thereof using the present invention and standard, well-known extended-state modeling techniques applicable to binary logic."* The Examiner assert that the current claim language does not reference the term *"FAST 14"* nor does it disclose the limitations that distinguish the current claim language over the prior art of record. The Examiner asserts that the Appellant is attempting to read limitations from the specification into the claim language and not employing *"means for"* language to do so, *(see In re Van Geuns (CA FC)26*

USPQ2d 1057). The Examiner asserts that if the current claim language contained limitations, as referred to by the Appellant in the specification, then the claims would be allowable over the prior art of record. Specifically, if the claims language used the term, *"FAST 14"*, then the claims would be distinguished over the prior art of record.

On page 9 of the Brief the Appellant has stated, *"In contrast, the present invention discloses a simulation model and methodology for non-binary logic that includes the "complete algebra" to enable the simulation that was out of the scope of the Rozen's article."* The Examiner asserts that if some of the mechanics of that *complete algebra"* were disclosed in the current claim language or if *means for* language where in the claims then the Appellant would be correct but, the current state of the claims language reads to a *"non-binary"*, *"N-NARY"* modeling system, where the term *"non-binary"* could easily be interpreted as meaning any simulation model where more that two states can be modeled, the term *"N-NARY"* could be interpreted to mean, *binary* if N equals 2, *tri-nary* if N equals 3, etc... The Examiner assert that the term *N-NARY* could be confused with other multi-valued logic systems *(see "On the Use of VHDL as a Multi-Valued Logic Simulator, pages 110&111).*

On page 10 of the Brief the Appellants have stated, *"The present application discloses that designers attempting to employ extended-state simulations for complex binary logic have developed workaround solutions, such as mapping large truth table functions to multiple smaller truth table functions, or ignoring certain states within a multiple state model for certain designs. Application at p.6, lines 16-20."* The Examiner asserts that, again, the Appellant is attempting to read limitations into the current claim language from the specification without using, *means for,* language. The Examiner asserts that, the current claim language, does not contain the word

mapping, and that there is nothing in the current claim language that discloses the limitation of, *mapping large truth table functions to multiple smaller truth table functions, or ignoring certain states within a multiple state model for certain designs.*

The Examiner asserts that the *Giramma (U.S. Patent 5,706,476)* reference does disclose, a signal model, **(Col. 1 Lines 32-50)**, as used in an N-NARY logic simulation, **(Figures 2&3 and Col. 1 Lines 51-62, Col. 7 Lines 7-22)** a signal value, **(Table 2 *note the Decimal Value column*, Col. 6 Lines 6-19)** of a non-binary 1-of-N logic signal being modeled where the logic value further comprises an integer greater than 1, **(Col. 6 Lines 51-67, Col. 7 Lines 1-7)** a signal strength, said signal strength comprises the drive state of said nonbinary **(Table 2 *note the Decimal Value column*)** 1-of-N logic signal being modeled, **(Col. 4 Lines 59-67, Col. 5 Lines 1-13)** a signal definition, said signal definition further comprises the defined or undefined status of said 1-of-N logic signal being modeled **(Col. 4, Lines 53-55)** although not present in the claim language, the *Giramma* reference discloses *mapping* of the logic values **(Figure 3 ITEM 106b).**

On page 11 of the Brief the Appellant has stated, *"Rozen does not include accounting for different driver strengths (i.e., strongly-driven, moderately-driven, weakly-driven) of his non-binary signals."* The Examiner asserts that, *by Appellant's own admission,* the *Rozon* reference discloses non-binary signals, the Examiner further asserts that, in Table 1 on page 110 of the *Rozen* reference is listed the terms, *(weak unknown, weak zero and weak one).* The Examiner asserts that these terms refer to signal strengths.

The Examiner asserts that the Appellant is confused as regards the lexicon of terms being used, specifically on page 11 of the Brief the Appellant states, *"In Applicant's lexicon as applied to a binary signal, the phrases "logic value" and "decimal value" refer only to the true-or-false,*

high-or-low, 1-of-0 nature of the signal—the information used to determine whether a binary signal is asserted or not. The Appellant then declares, *"In Applicant's lexican, a signal's "logic value" or "decimal value" bears no relation to its drive state or whether the signal has a status other than asserted or not asserted (i.e., whether a signal is undefined, unitialized, or high-impedance).* The Examiner asserts that he is unsure what the term *1 of 0* is supposed to represent. The Examiner is unsure what distinction Appellant was trying to make between the claimed invention and the prior art. The Examiner asserts that the Appellant intended to present one set of lexicon's as being that of the Examiner and the other as that of the Appellant.

On page 13 of the Brief the Appellant states, *"Unfortunately, despite this explanation, the Examiner continues to mischaracterize the ability of prior art models to simulate various signal characteristics of binary signals...).* The Examiner asserts that there is no effort to mischaracterize Appellant's invention over the prior art of record. The Examiner asserts that the current claim language does not overcome what is disclosed in the prior art of record. The Examiner asserts that if the Appellant had amended the current claim language to include the term *"FAST 14"*, which is a trademark of Appellant's assignee, then the confusion concerning the prior art of record and the current claim language would be reduced.

On page 15 of the Brief the Appellant states, *"While that may be true as an abstract principal, Applicant has clearly defined and used the term "drive state" to refer only to the strength of a signal, independent of its value."* The Examiner asserts that there is no language in the claims that distinguishes between the *drive strength* of a signal being *independent of its value*. The Examiner asserts that there is no distinction made in the current claims language regarding the independence of these two elements of modeling the signal, for example, from

Claim 6, *"assigning a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled"* the Examiner fails to see the distinction being made by the Appellant that there is independence between the *signal value* of the same claim and the *signal strength* as disclosed in claim 6.

On page 17 of the Brief the Appellant states, *"Giramma's model, is not the same as the model of the present invention, because the present invention models multiwire 1-of-N signals."* The Examiner asserts that the term *multiwire* does not appear in any of the claims.

On page 18 of the Brief the Appellant states, *"Applicant does not dispute that Giramma teaches propagating a modeled signal that has a signal value."* The Examiner asserts that the Appellant is correct in that the *Giramma* reference discloses the claimed limitations as they are disclosed at this time.

On page 18 of the Brief the Appellant states, *"1-of-N logic signals are specifically defined in the specification to be multiwire signals..."* The Examiner asserts that there is no, *means for* language in the claims to provide this support and that the term, *multiwire* does not appear in the claim language.

On page 19 of the Brief the Appellant states, *"As before, Giramma does not teach the functional limitations of the claimed signal definition element: it must comprise the defined or undefined status of the nonbinary 1-of N logic signal being modeled."* The Examiner asserts that the *Giramma* discloses the term *undefined,* ***(Giramma, Col. 4 Lines 53-55)*** in reference to a signal state.

On page 20 of the Brief the Appellant states, *"the Examiner has confused the ability to model states of a binary signal with the ability of the present invention to model multiple states*

of a non-binary, multiwire 1-of-N signal." The Examiner asserts that the word *multiwire* does not appear in the amended claim language. The Examiner asserts that the distinction that Appellant has drawn between the (IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164)) is not reflected in the current claim language and that the Examiner has determined that 1-of-N signal could be interpreted as meaning 1-of-2 signals for simple binary representation, or say 1-of-3 signals for either a logic "1" or logic "2" or logic "x" where "x" is a, *don't care* state as used in Karnaugh maps, *(please refer to pages 72 and 167-170 of "Digital Design" by M. Morris Mano, California State University, Los Angeles, Prentice Hall, 1984).*

On page 21 of the Brief the Appellant states, *"...because the reference does not teach the modeling of a nonbinary 1-of-N signal, the reference does not teach the claimed signal strength that is limited to being the drive state of a 1-of-N signal."* The Examiner asserts that a *nonbinary 1 of N signal* is any signal that has more than 2 possible values and that 1-of-N refers to the 1 or N possible signal representations so that, for example, a system of modeling signals, as disclosed in the *IEEE* reference is a *nonbinary, i.e. there is a possibility of more that 2 values for a given signal, further, the signal could not only be a logic low, or 0 but might be a weak logic low signal, so this would be a nonbinary 1 of 2, where N is 2, signal because it could be a normal logic 0 or a weak logic 0.*

On page 22 of the Brief the Appellant has argued that, *"Applicant has decided upon a description style that, contrary to Rozon's assertion, accounts for signal drive strengths without increasing the model's complexity."* The Examiner asserts that the Appellants current claim language does not support a distinction over the elements disclosed in the *Rozon* reference.

On page 22 of the Brief the Appellant has argued that, *"Rozon's signals do not have drive strength."* The Examiner asserts that in Table 1 on page 110 of the *Rozen* reference the terms, *weak unknown, weak zero and weak one* denote drive strength.

On page 23 of the Brief the Appellant has argued that, *"Examiner cites page 112 and Table 2 as teaching a signal definition. In fact, this table has nothing to do with a signal model that includes a signal definition that comprises the defined or undefined status of a binary 1-of-N logic signal being modeled."* The Examiner asserts that, after reconsideration, that the Appellant is correct and the earlier 35 U.S.C. 102(b) rejection of **Claims 1-3, 6-8, 11-13, 16-18 and 21-23** as being clearly anticipated by "On the Use of VHDL as a Multi-Valued Logic Simulator" by C. Rozon, IEEE 1996 hereafter referred to as the **Rozon** reference is withdrawn.

On page 24 of the Brief the Appellant has argued that, *"For the same reasons discussed above, the signal models disclosed by Giramma, IEEE_Std_logic_1164, and Rozon do not teach, suggest, or imply a signal model that includes all the claimed elements and limitations in claim 1.)* The Examiner asserts that the *Giramma* reference discloses signal models **(Col. 1 Lines 35-50).**

On page 24 of the Brief the Appellant has stated, *"Applicant has explained to the Examiner, Giramma's 32-bit zoom words have nothing to do with the logic value of a modeled signal."* The Examiner asserts that 32-bit *"zoom"* words have to do with are used to obtain indices into various tables for next-state logic evaluations **(*Giramma* Col. 6 Lines 51-66)**, they are representations in memory for a particular logic signal and it possible future value. The Examiner asserts that this is directly related to logic value of a modeled signal.

On page 25 of the Brief the Appellant argues that, *"Giramma maps the binary output of one primitive gate—say, an OT gate—from a signal model that may represent any one of 8 characteristic states of the output binary signal to a signal model that may represent any one of 4 characteristic states for the next downstream primitive gate."* Then on page 26 of paper #11 the Appellant argues, *"Next, the "essence" of Applicant's invention is not "to abstract several signal wires into one 32 bit word and represent an "N-Nary" set of modeled logic signals." Once again, this statement demonstrates a fundamental laock of understanding of Applican'ts FAST14 technology."* The Examiner asserts, again, that the current claim language does not disclose multiple wires and the term *FAST 14* does not appear and therefore the *Giramma* reference reads on the current state of the amended claims.

On page 27 of the Brief the Appellant argues that, *"Applicant directs the Examiner's attention to ...Assignee's well-defined FAST 14 technology."* The Examiner asserts that the term *Fast14* does not appear in the amended claim language.

On page 28 of the Brief the Appellant has stated, *"Applicant does not dispute that the signal models disclosed in Giramma and the IEEE reference teach modeling drive strengths of the binary signals that they model."* The Examiner asserts that these are not *binary* signals but *N-Nary* signals because they can have more than two values, *see discussion above.* The Examiner asserts that, *by Appellants own admission,* the *IEEE* reference teaches signals models that have drive strengths.

On page 31 of the Brief the Appellant states, *"The behavioral model includes an input logic signal reader 30 that reads validity, value, and drive strength..."* this statement was made in regards to U.S. Patent 6,289,497 which is used in the non-statutory double patenting rejections

of the amended claims. Further on page 31 of the Brief, when describing the current application under consideration the Appellant states, *"The signal model of the present invention defines a particular signal's specific characteristics such as the specific logic value, drive strength, and defined/undefined status at a particular point in time."* The Examiner asserts that based on this admission, and the earlier rejection of the claims based on the Judicially created doctrine of non-statutory double patenting that these two sets of claims are an obvious variation of each other.

On page 33 of the Brief the Appellant states, *"...the evaluation field, and the clock phase field, because the N-NARY design tool requires that information to produce the circuit schematic and behavioral model. Without these pieces of information, that tool would not "know" the width (i.e., how many conductors) of a specified signal, whether it is a signal internal to a gate or a signal that connects gates, or what phase clock that gate that drives the specified signal needs."* The Examiner asserts that none of the distinctions concerning the *design* tool needing to *know* the width or *how many conductors* of the *specified signal* is disclosed in the claim language of *Leight et al.* U.S. Patent 6,289,479. The Examiner asserts that *Leight et al.* reference is an obvious variation of the Appellants currently amended claim language *(see the non-statutory double patenting rejection above)*.

On page 34 of the Brief the Appellant argues that, *"The '497 claims do not teach a signal strength that comprises the drive state of a nonbinary 1-of-N logic signal..."* The Examiner asserts that the *signal degree field* as disclosed in the *Leight et al.* reference's claims would be interpreted by one of ordinary skill in the art, at the time of the invention, be understood to be the degree of *signal strength of a modeled signal.* The Examiner asserts that in Claim 6 of the *Leight*

et al. reference is disclosed that the signal naming convention is for N-nary logic circuits, which are *nonbinary 1-of-N logic signals* by definition.

Summary

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
Dwin McTaggart Craig

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August 25, 2003

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Application No. 09/405,618

Art Unit 2123

The remand, paper # 15 has been responded to.

The Examiner respectfully requests that the following correction to the original Examiner's Answer be entered.

Please substitute old page 3 with the new page 3.

Summary

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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February 9, 2004

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(9) Prior Art of Record

5,706,476	Giramma	1-1998
6,289,497	Leight et al.	11-2001

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